REMARKS/ARGUMENTS

Claims 1-18 remain in this application. Claims 20-28 have been withdrawn as the result of an earlier restriction requirement. Applicants retain the right to present Claims 19-29 in a divisional application.

I. THE REJECTION UNDER 35 U.S.C. §102

The examiner rejected claims 1, 2, 4, 10-13, 17 and 18 under 35 U.S.C. 102(b) as being anticipated by Distefano et al., US Patent No. 5,834,339. The examiner argues that Figure 2F of Distefano et al. teaches the system of the present invention.

Distefano is directed toward "the pressure injection of encapsulants into cavities and gaps in microelectronic structures and the simultaneous removal of voids and gas bubbles within encapsulants and adhesive/chip attach layers." (Col. 5, lns. 39-43) Figure 2F illustrates a carrier 285 that may be used to perform the "injection methods ... on more than one assembly at a time to facilitate the mass production of finished parts." (Col. 9, lns. 40-42) Neither the carrier 285 of Figure 2F nor the frame assemblies 221, incorporating frame 280, within carrier 285 are part of the finished product created via the Distefano method. In fact, frames 280 are removed from the carrier 285 and then separated into "single packaged chips." (Col. 10, lns. 32-35) Thus Figure 2F teaches one of skill in the art a way to temporarily arrange the chips so that multiple chips may be placed within a pressure chamber at the same time during their fabrication. Nothing in the Distefano patent, particularly in Figure 2F, teaches or implies that carrier 285 and/or frames 280 may be used as a permanent packaging system for the chips. Hence, Figure 2F does not describe a final three-dimensional packaging of platelets, such as computer chips, as described and claimed in the present application.

The present invention "relates to three-dimensional circuit packages ... for semiconductor platelets." (Pg. 2, lns. 6-8). Three-dimensional integrated circuits are a final product in and of themselves and are employed in applications in which space is a critical design factor. (Pg. 2, lns. 11-12) The present invention teaches a system for packaging these three dimensional circuits that provides tight spacing tolerances between the platelets and minimizes the damage to the platelets during the packaging process. (Pg. 3, lns. 17-19) Claim 1 has been amended to more clearly reflect that the system of the present invention is for the final "three-dimensional packaging" of the integrated circuits and not merely a temporary stacking arrangement used during the production of individual computer chips.

Clearly, Distefano et al. cannot anticipate the present invention because it does not teach a system for three-dimensional packaging as taught in the present invention.

II. THE REJECTIONS UNDER 35 U.S.C. §103

A. The Rejection of Claims 3 and 5-9 Over Distefano et al. in view of Vafai

The examiner rejected Claims 3 and 5-9 as being unpatentable over Distefano et al., US Patent 5,834,339, as applied to claims 1 and 2 above, and further in view of Vafai, US Patent 6, 457,515. The examiner argues that Vafai "teaches the use of silicon as a heat sink material."

As described in detail in Section I above, Distefano et al. does not teach a system for three-dimensional packaging as taught in the present invention. Furthermore, Distefano cannot suggest or render obvious the system of the present invention because Distefano only teaches a temporary arrangement of components during a single step in a fabrication process of single computer chips. Regardless of whether or not Vafai "teaches the use of silicon as a heat sink material," even if one of skill in the art were to combine the teachings of Distefano and Vafai, he would still not arrive at the system of the present invention. Thus the combination of Distefano and Vafai cannot possibly render the present invention obvious.

B. The Rejection of Claims 14-16 Over Distefano et al. in view of King et al.

The examiner rejected Claims 14-16 as being unpatentable over Distefano et al., US Patent 5,834,339, as applied to claim 1 above, and further in view of King et al., US Patent 5,140,405.

The examiner argues that King teaches "a semiconductor assembly comprising a chip carrier having a floor (40) and a frame (42) (Figure 6)." While the Applicant disagrees that the semiconductor assembly taught by King is equivalent to the platelets taught by the present invention, irrespective of this disagreement, it is undisputed that the teachings of King do not overcome the insufficiencies of Distefano as described in Section I above. Furthermore, King does not suggest or obviate the system for three-dimensional packaging of the present invention. The use of the invention of King in the invention of Distefano would not render obvious the present invention.

Respectfully submitted,

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